

**REMARKS**

Claims 1-10, 13 and 14 are pending in the application. Claims 1, 13 and 14 are rejected.

**Claim Rejections - 35 U.S.C. §102**

Claims 1 and 14 are rejected under 35 U.S.C. §102(b) as being anticipated by Olsen (EP 926715).

Applicants respectfully disagree with this rejection, and traverse it for the following reasons.

Initially, Applicants note that the step “etching the first film by using the second film as a mask” was argued by the Examiner to have been inherently performed by Olsen, because although the second film and first film are etched at the same time, the second film would necessarily be etched, and then the first film would be etched “using the second film as a mask”. Applicants do not agree with this somewhat creative interpretation of the process steps of Olsen.

Applicants note that the web site [www.chemindustry.com](http://www.chemindustry.com) defines a semiconductor mask as, “*a thin template of metal or another material used to shield parts of a semiconductor during an etching or deposition process*”. Because the phrase “used to shield” clearly implies that some areas under the “mask” are intended to remain after the etching step, which is not the case in Olsen. Applicants submit that that one skilled in the art would immediately interpret the claimed step of “etching the first film by using the second film as a mask” as preparing a patterned first film by use of a pattern of a second overlying film; however, this is not the case in Olsen. Therefore, Olsen does not teach or suggest “using the second film *as a mask*”.

More importantly, the present claim 1 recites the step of “ashing and removing the resist film” immediately before the step of “etching the first film by using the second film as a mask”. Applicants note no teaching or suggestion in the cited reference to perform this step, and submit that this limitation is also not met by the cited reference.

Because claim 14 is properly dependent from and necessarily includes at least the limitations from claim 1, Applicants disagree with the rejection of claim 14, as well.

### **Claim Rejections - 35 U.S.C. §103**

Claim 1 is rejected under 35 U.S.C. §103(a) as being unpatentable over Passemard (U.S. Patent No. 6,624,053) in view of Rind (U.S. Patent No. 6,475,889). The Examiner admits that Passemard is silent on the gas mixture used to etch the second film and does not disclose that the second film of silicon carbide is etched using a fluorocarbon gas added with one of SF<sub>6</sub> and NF<sub>3</sub>. The Examiner concludes that it would have been obvious to etch the silicon carbide (second film) in the method of Passemard using a fluorocarbon gas added with one of SF<sub>6</sub> and NF<sub>3</sub> because Ring teaches that conventionally silicon carbide is etched using NF<sub>3</sub> or SF<sub>6</sub> diluted with AR and CF<sub>4</sub>/O<sub>2</sub>.

Claim 13 is rejected under 35 U.S.C. §103(a) as being unpatentable over Olsen or Passemard in view of Ring as applied to claim 1 above, and further in view of Dabbaugh (U.S. Patent No. 6,362,094). The Examiner admits that the references do not disclose that the silicon carbide film is deposited by CVD using tetramethylsilane and carbon dioxide in a flow rate ration of 0.2 to 0.6. The Examiner concludes that it would have been obvious to deposit the silicon carbide layer by CVD using tetramethylsilane and carbon dioxide because Dabbaugh teaches that this is a known method for deposition of hydrogenated silicon carbide. Dabbaugh is

silent on the flow rates of the source gases and does not disclose that the tetramethylsilane and the carbon dioxide flow rates are in a ration of 0.2 to 0.6. It would within the ordinary skill of one in the art to determine the optimal flow rates ratio for the tetramethylsilane and carbon dioxide in the methods above by routine experimentation and to have the ratio be 0.2 to 0.6, if required, because source gas flow rates are result effective variables and the discovery of an optimum value of a result-effective variable is ordinary within the skill of the art.

Applicants respectfully disagree with and traverse the rejection of claims 1 and 13 under 35 U.S.C. §103 for the same reasons as described above. That is, the steps of "ashing and removing the resist film" and "etching the first film by using the second film as a mask" are not met by the cited references, either alone or in combination. Applicants therefore traverse the rejection of claim 1.

Because claim 13 is properly dependent from and necessarily includes at least the limitations from claim 1, Applicants disagree with the rejection of claim 13, as well.

In view of the aforementioned remarks, Applicants submit that that the claims are in condition for allowance. Applicants request such action at an early date.

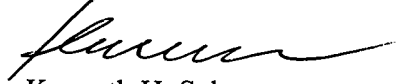
If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

Response under 37 C.F.R. §1.111  
Attorney Docket No. 020060  
Serial No. 10/058,426

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

**WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP**



Kenneth H. Salen  
Attorney for Applicants  
Registration No. 43,077  
Telephone: (202) 822-1100  
Facsimile: (202) 822-1111

KHS/ldc

Enclosure: "semiconductor mask", [www.chemindustry.com](http://www.chemindustry.com) definition

**BEST AVAILABLE COPY****Chem  
Industry.com**

[find your site] [subscription center] [advertiser login] [about us] [home]

.....The worldwide search engine of the chemical industry

[expert home](#) | [request a project](#) | [about us](#) | [help](#)[semiconductor mas](#)[go](#)[search tips](#)**Search Results for 'semiconductor mask'**

Definition: A protective mask that is a thin template of metal or another material used to shield parts of a semiconductor during an etching or deposition process.

**Related Search Terms**

[-hard semiconductor mask](#)  
[-soft semiconductor mask](#)  
[-semiconductor mask](#)  
[-contact aligner](#)  
[-photoresist](#)  
[-semiconductor lithography](#)  
[-microlithography](#)  
[-semiconductor device](#)  
[-etching](#)  
[-semiconductor material processing](#)  
[-semiconductor sililation](#)  
[-photoresist stripping](#)  
[-semiconductor wafer mask aligner](#)  
[-semiconductor dopant lateral diffusion](#)  
[-ion-beam etching](#)  
[-etch pit density](#)  
[-etching material](#)  
[-etch rate](#)  
[-photochemical etching](#)  
[-lift-off \(semiconductor fabrication\)](#)

**Experts -  
1 to 5 of 5****Expert  
107629****Expert  
720603****Expert  
722748****Expert  
108092****Expert  
107923****Expertise**

Scanning Electron and Light Microscopy, EBEAM Lithography and Nanofabrication

Semiconductor Processing and Equipment

Advanced Semiconductor Technology Intellectual Property and Licensing

Semiconductor Manufacturing

Semiconductor Processing Technology

**View  
Bio**[View Bio](#)**Request a  
Project**[Request a Project](#)[View Bio](#)[Request a Project](#)[View Bio](#)[Request a Project](#)[View Bio](#)[Request a Project](#)[View Bio](#)[Request a Project](#)

©2005 Teltech, A Division of FIND/SVP, Inc. All Rights Reserved.

[Privacy Policy](#)